METHOD OF FORMING A CMOS TRANSISTOR

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a manufacturing method of forming a CMOS transistor, and more particularly to a manufacturing method of forming the source/drain and lightly doped region of a CMOS transistor using two procedures of implantation.

Description of the Related Art

[0002] While most thin film transistors used in flat displays are manufactured via amorphous silicon manufacturing process, only a few advanced products adopt polysilicon manufacturing process which has higher electron mobility. Polysilicon technology allows more electronic circuits to be integrated into, so the overall complexity and weight of product can be reduced. Since the highest temperature during polysilicon manufacturing process is over 300^0 C, a temperature far above the softening point of plastics,

so this manufacturing process can only be applied to glass substrate.

[0003] Referring to FIG. 1A ~ 1I, diagrams showing a conventional manufacturing process of a low-temperature polysilicon thin film transistor. Firstly, in FIG. 1A, a buffer layer 102 and a polysilicon layer 104 are sequentially formed on a substrate 100, wherein the polysilicon layer is formed by using excimer laser to crystallization anneal the amorphous layer. Next, a patterned photoresist layer is formed (not shown here) and the polysilicon layer 104 as shown in FIG. 1A is formed thereafter by using the photoresist layer as a mask of etching process.

[0004] After that, referring to FIG. 1B, a gate oxide 108 is deposited over buffer layer 102 and polysilicon layer 104; a conductive layer is further formed over gate oxide 108. Gate 110 is then formed by using photolithography and etching process. Following that, in FIG. 1C, a photoresist layer 112 which covers up entire PMOS transistor region as well as the gate and lightly doped region of NMOS transistor is formed. Furthermore, photoresist layer 112 is used as mask and a high concentration phosphorus dopant is implanted to form the source/drain 104a, 104b, 104c, and 104d of NMOS transistor.

[0005] Following that, in FIG. 1D, the remnants of photoresist layer 112 are removed, gate 110 is used as mask directly, and a low concentration

phosphorus dopant is implanted into substrate 100 to form the lightly doped regions 104m, 104n, 104x, and 104y of NMOS transistor. Next, in FIG. 1E, a photoresist layer 114 is formed again, wherein the photoresist layer 114, which covers up entire NMOS transistor region, is used as mask, and a high concentration boron dopant is implanted into substrate 100 to form the source/drain 104i and 104j of P-type transistor.

[0006] In FIG. 1F, first of all, the photoresist layer 104 is removed, an inner dielectric layer 116 is formed on gate 110 and gate oxide 108 with a plurality of openings are formed in inner dielectric layer 116 and gate oxide 108. Next, in FIG. 1G, an electrode 118 which can be electrically connected to source/drain 104a, 104b, 104c, 104d, 104i, and 104j is formed therein.

[0007] Next, in FIG. 1H, a passivation layer 120 is formed on electrode layer 118 and inner dielectric layer 116, wherein an opening is formed on passivation layer 120 of pixel region so that electrode 118 can be exposed. Lastly, in FIG. 1I, a transparent electrode 122 which can be electrically connected to electrode 118 of pixel region is formed so as to conclude the manufacturing process of low-temperature polysilicon thin film transistor.

[0008] The manufacturing process of low-temperature polysilicon thin film transistor according to the conventional technology requires eight

photo-masking and three procedures of ion implantation, wherein the eight processes of masking are illustrated in FIG. 1A ~ 1C and FIG. 1E ~ 1I while the three procedures of ion implantation are illustrated in FIG. 1C ~ 1E. However, each manufacturing procedure adds to an increase in manufacturing cost. It is therefore an urgent need to reduce the required number of manufacturing procedures if the manufacturing cost is to be further cut down.

SUMMARY OF THE INVENTION

[0009] It is therefore an object of the invention to provide a manufacturing method of forming a CMOS transistor using less manufacturing procedures.

[0010] It is therefore an object of the invention to provide a method of forming a Type-I transistor and a Type-II transistor suitable for liquid crystal display (LCD). The method comprises the following procedures: providing a substrate; forming a first polysilicon layer and a second polysilicon layer corresponding to the Type-I transistor and the Type-II transistor respectively on the substrate; blanketly forming a gate insulating layer on the first polysilicon layer, the second polysilicon layer, and the substrate; forming a first gate and a second gate on the gate insulating layer respectively corresponding to the first polysilicon layer and the second polysilicon layer;

performing a first doping using a first type dopant to form a first heavily doped region in the first polysilicon layer beside the first gate; and performing a second doping using a second type dopant to simultaneously form a second heavily doped region in the second polysilicon layer beside the second gate and form a lightly doped region in parts of the first heavily doped region beside the first gate, wherein the dosage of the second type dopant is smaller than that of the first type dopant.

[0011] Following the step of forming a lightly doped region of the Type-I transistor and a second heavily doped region of the Type-II transistor, the invention further comprises the following procedures: First, forming a 500 ~ 700 angstrom thick inner dielectric layer on the gate oxide, the first gate and the second gate; second, selectively exposing the first heavily doped region, the second heavily doped region, the first gate and the second gate; third, forming an electrode includes either of Mo, Cr, and Ti/Al/Ti to be electrically connected to the exposed first heavily doped region, second heavily doped region, first gate and second gate.

[0012] Following the step of forming the electrode, the invention further comprises the following procedures: First, forming a patterned passivation layer on the inner dielectric layer and the electrode, wherein the patterned passivation layer exposes part of the electrode of the Type-I transistor situated

in pixel region. Second, forming a transparent electrode including indium-tin oxide (ITO) to be electrically connected to the exposed part of the electrode of the Type-I transistor.

[0013] In the invention, the Type-I transistor is an NMOS transistor while the Type-II transistor is a PMOS transistor, wherein the first type dopant is a phosphorus dopant while the second type dopant is a boron dopant; or alternatively, the Type-I transistor is a PMOS transistor while the Type-II transistor is an NMOS transistor, wherein the first type dopant is a boron dopant while the second type dopant is a phosphorus dopant.

[0014] Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1A ~ 1I are diagrams showing the manufacturing process of a conventional low-temperature polysilicon thin film transistor; and

[0016] FIG. 2A ~ 2H are diagrams showing the manufacturing process of a low-temperature polysilicon thin film transistor suitable for liquid crystal display

(LCD) according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The invention provides a manufacturing process of low-temperature polysilicon thin film transistor with fewer steps.

[0018] Referring to FIG. 2A ~ 2H, these diagrams show the manufacturing process of a low-temperature polysilicon thin film transistor suitable for liquid crystal display (LCD) according to the invention. First of all, in FIG. 2A, a buffer layer 202 and a polysilicon layer are sequentially formed on a substrate 200. Next, a patterned photoresist layer (not shown here) is formed on the polysilicon layer, and the photoresist layer is used as a shield during etching process to form a polysilicon layer 204(1), 204(2), and 204(3) shown in FIG. 2A.

[0019] Substrate 200 according to the invention can be made of glass or plastics. Polysilicon layer 204(1), 204(2), and 204(3) with the thickness of about 200 ~ 1000 angstroms are formed by crystallization annealing an amorphous silicon layer on buffer layer 202 by using excimer laser. The polysilicon layers 204(1) and 204(2) at the left are used to form a first NMOS

transistor and a first PMOS transistor, which consist of a CMOS transistor, while the polysilicon layer 204(3) at the right is used to form a second NMOS transistor situated in pixel region of the LCD.

[0020] Buffer layer 202 can comprise a silicon oxide or a silicon nitride and is used as an isolating layer during the excimer laser annealing process. For example, despite the upper polysilicon layer 204 may reach a temperature as high as 1500^{0}C during annealing, the regional temperature of a plastic substrate will not exceed 250^{0}C. Furthermore, the regional temperature stays at high levels only for a short while, so the plastic substrate will not be deformed.

[0021] Referring to FIG. 2B, a gate insulating layer, for example, a gate oxide 208, which can comprise SiO_2 with a thickness of 500 ~ 1500 angstroms, is blanketly formed on the buffer layer 202, the polysilicon layer 204(1), 204(2), and 204(3), and the substrate 200. Next, a conductive layer is deposited on the gate oxide 208, and gate 210(1), 210(2), 210(3), which can include Mo, Cr, or Ti/Al/Ti, are formed using photolithography and etching process. The gate 210(1), 210(2), 210(3) respectively correspond to the polysilicon layer 204(1), 204(2), and 204(3).

[0022] After that, in FIG. 2C, a patterned photoresist layer 212 is formed on

substrate 200 through photolithography, wherein photoresist layer 212 covers up entire first PMOS transistor region which may form a CMOS transistor. Furthermore, photoresist layer 212 is used as a mask and a high concentration phosphorus dopant is implanted into substrate 200 to form heavily doped regions 204A, 204B, 204C, and 204D on the source/drain and lightly doped region of the first and second NMOS transistors, wherein the dosage of the phosphorus dopant is about 3el3 dosage/cm^2 ~ 5el5 dosage/cm^2. Meanwhile, the part of the source/drain region of the first and second NMOS transistors formed by heavily doped regions 204A, 204B, 204C, and 204D is exactly the source/drain of the first and second NMOS transistors. The heavily doped region 204A and 204B in the polysilicon layer 204(1) are formed beside the first gate 210(1), while the heavily doped region 204C and 204D in the polysilicon layer 204(3) are formed beside the first gate 210(3). This will be further elaborated after the procedures in FIG. 2D are completed.

[0023] After that, in FIG. 2D, the remnants of photoresist layer 212 are removed and a patterned photoresist layer 214 is formed on gate oxide 208 through photolithography, wherein photoresist layer 214 covers up the source/drain region of the first NMOS transistor of the CMOS transistor as well as the source/drain region of the second NMOS transistor in pixel region, but not the first PMOS transistor region of the CMOS transistor. Furthermore,

photoresist layer 214 is used as a mask and a high concentration boron dopant is implanted into substrate 200 to form heavily doped region 204i and 204j, the source/drain of the first PMOS transistor, as well as lightly doped regions 204m, 204n, 204x and 204y respectively in parts of the heavily doped region 204A, 204B, 204C, and 204D of the first and second NMOS transistors, wherein the dosage of boron dopant is about 3el3 dosage/cm^2 ~ 5el5 dosage/cm^2. The heavily doped regions 204i and 204j in the polysilicon layer 204(2) are formed beside the gate 210(2), the lightly doped regions 204m and 204n are formed beside the gate 210(1), and the lightly doped regions 204x and 204y are formed beside the gate 210(3). In heavily doped regions 204A, 204B, 204C, and 204D, the part other than lightly doped regions 204m, 204n, 204x, and 204y is exactly source/drain 204a, 204b, 204c and 204d of the NMOS transistor.

[0024] It is noteworthy that the dosage of the boron dopant must be smaller than that of the phosphorus dopant implanted in order to produce lightly doped regions 204m, 204n, 204x and 204y of the NMOS transistor after the two procedures of boron dopant implantation and phosphorus dopant implantation. However, the invention is not limited to the NMOS transistor with lightly doped regions. A PMOS transistor with lightly doped regions can be another embodiment of the invention. When this is the case, boron

dopant is implanted if photoresist layer 212 is used as a mask while phosphorus dopant is implanted if photoresist layer 214 is used as a mask, wherein the dosage of the boron dopant implanted must be greater than that of the phosphorus dopant implanted.

[0025] Next, in FIG. 2E, an inner dielectric layer 216 is formed on the entire substrate 200 after photoresist layer 214 is removed, and further a number of openings are formed in inner dielectric layer 216 and gate oxide 208 using photolithography and etching process, wherein inner dielectric layer 216 can include SiO_2 with a thickness of 500 ~ 7000 angstroms. After that, in FIG. 2F, a conductive layer is formed over the inner dielectric layer 216. The conductive layer fills up the openings in inner dielectric layer 216 and gate oxide 208; and further photolithography and etching process are performed to form electrode 218 which can be electrically connected to gate 210(1) ~ (3) and part of source/drain 204a, 204b, 204c, 204d, 204i and 204j. This embodiment illustrates the electrical connection between electrode 218 and source/drain 204a, 204b, 204c, 204d, 204i and 204j.

[0026] Following that, in FIG. 2G, a passivation layer 220 is formed on electrode 218 and inner dielectric layer 216 and an opening in passivation layer 220 in pixel region is formed through photolithography and etching process. Last, in FIG. 2H, a conductive layer including ITO 220 is formed in

passivation layer 220. The conductive layer fills up the opening therein, and further photolithography and etching process are applied to form a transparent electrode 222 which can be electrically connected to electrode 218 in pixel region to complete the manufacturing process of low-temperature polysilicon thin film transistor.

[0027] The manufacturing process disclosed in the above preferred embodiment only requires eight processes of masking and two procedures of ion implantation to form low-temperature polysilicon thin film transistor. Of which, the eight masking processes are performed in FIG. 2A ~ 2H, while the two ion implanting procedures are performed in FIG. 2C and FIG. 2D respectively. Generally speaking, the manufacturing method according to the invention requires one less procedure of ion implantation when compared with the conventional technology; hence the manufacturing cost is further cut down.

[0028] While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.